ALTERA STRATIX™ EP1S25 FIELD-PROGRAMMABLE GATE ARRAY (FPGA)

A.B. Sanders[1], K.A. LaBel[1], C. Poivey[2], Joel A. Seely[3]

1. NASA/GSFC, Code 561.4 Greenbelt, MD 20771
2. NASA/MEI, Greenbelt, MD 20771
3. Altera Corporation, San Jose, CA 95134

OUTLINE

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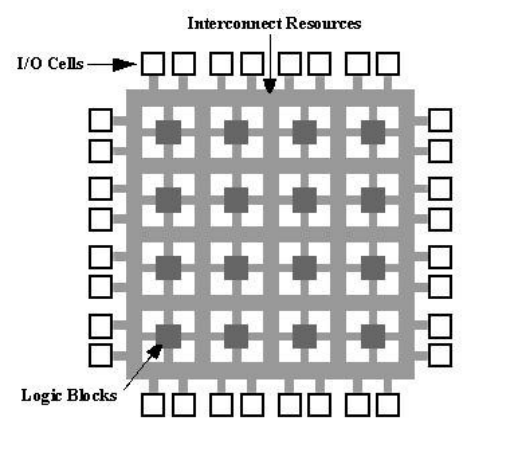
INTRODUCTION



INTERNAL FPGA

- Configurable Logic Blocks provide functional elements for constructing user's logic
- I/O Cells provide the interface between the package pins and internal signal lines
- Programmable Interconnect Resources provide routing paths to connect the inputs and outputs onto the appropriate networks
- Customized configuration is established by programming internal static memory cells that determine the logic functions and internal connections implemented in the FPGA

DEVICE CHARACTERISTICS

- **Characteristics:**
  - All Layer Copper SRAM Process
  - 1.5V, 0.13 µm CMOS Technology
  - 25,660 Logic Elements
  - Total Ram Bits = 1,944,576
  - 80 Embedded Multipliers
  - 6 Phase-Locked Loops
  - 706 Maximum User I/O pins

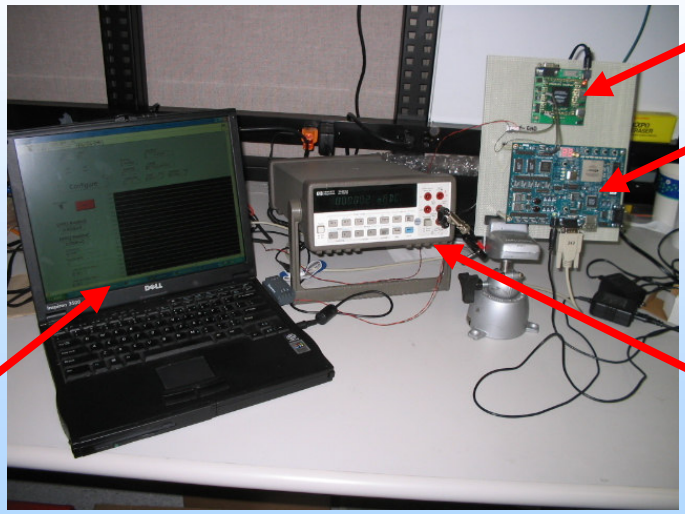
Columns / Blocks

Device	M512 Ram	M4K Ram	M-Ram Blocks	DSP Block	LAB Columns	LAB Rows
EP1S25	6 / 224	3 / 138	2	2 / 10	62	46

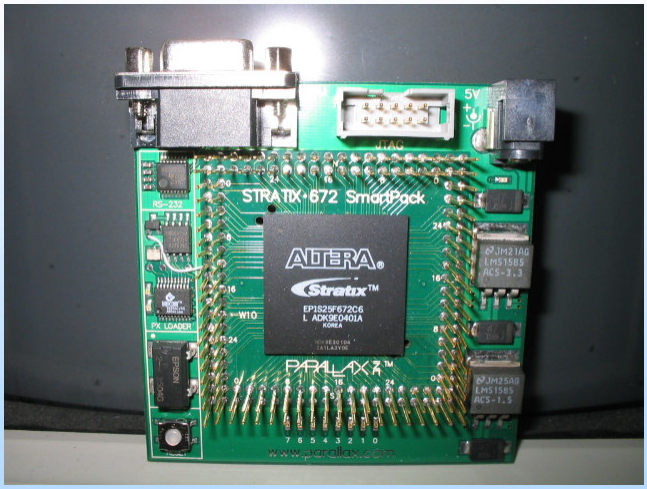
STRATIX FUNCTIONALITY

- **Stratix Devices:**
  - **Contain a two-dimensional row and column based architecture to implement custom logic. A series of interconnects of varying length and speed provide signal interconnects between logic array blocks (LAB), memory block structures, and DSP blocks.**
  - **Each LAB contains 10 logic elements (LE). An LE is a small unit of logic providing efficient implementation of user logic functions.**

RADIATION TEST SUITE

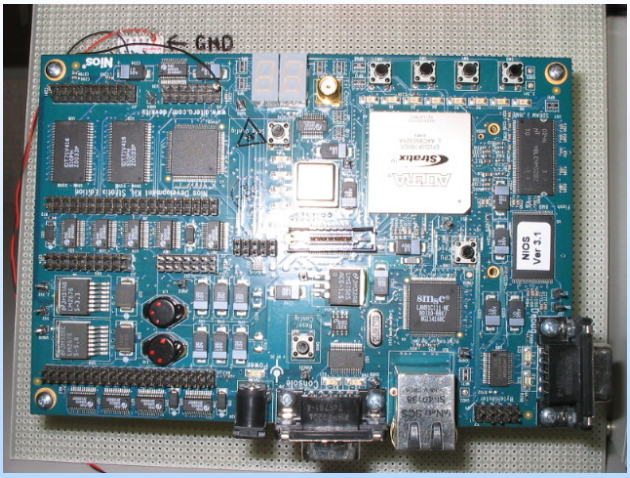


ALTERA DUT BOARD



ALTERA Device Under Test (DUT)

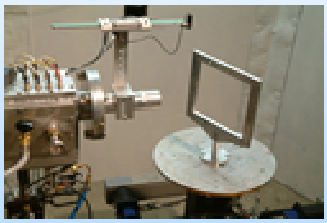
ALTERA DUT MONITORING BOARD



ALTERA Monitoring Board for control/data to the DUT

ION BEAM CHARACTERISTICS

Ion	Energy (MeV)	Angle (Degrees)	Range (μm)	Effective LET (MeV/(mg/cm²))
Ne	262	0	256	2.8



- **Orientation: Test fixture was oriented at an zero angle of incidence**

Altera Stratix Heavy Ion Testing at Room Temperature at TAMU

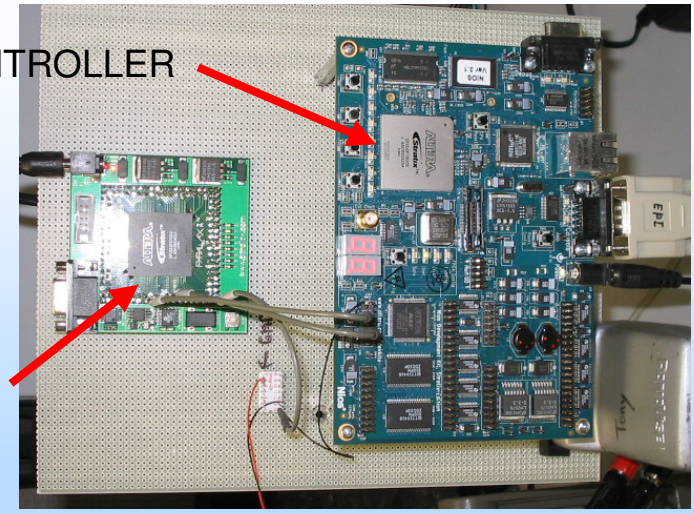
HYPERTERMINAL TEST CONFIGURATION

Configuration
115 kbps
8 data bits
1 stop bit
No parity
No hardware handshaking

Signal	Monitoring Board	DUT Board
GND	Pin 1 on J15	Any GND pin
RECONFIG_DUT	Pin 5 on J15	W13
CRC_ERROR	Pin 7 on J15	W20

ALTERA Stratix Heavy Ion SEU Test Programs at TAMU

BOARD INTERCONNECTIONS



Test Board in horizontal position with DUT Board on the left
using jumper wires for interconnection between the Monitoring Board

TEST PROCEDURE

- **Establish the correct test conditions**
- **Run the Hyperterminal and Labview programs to test the device with the proper configurations and verify test set functionality**
- **Irradiate the test device to the desired effective fluence while monitoring the device for SEE and SEU for proper health**
- **Check for output degradation and/or current increases to determine the number of upsets, latchup, or test anomalies**
- **Read the test device configuration to check for configuration SRAM errors**
- **Record all relevant test data from exposure run**

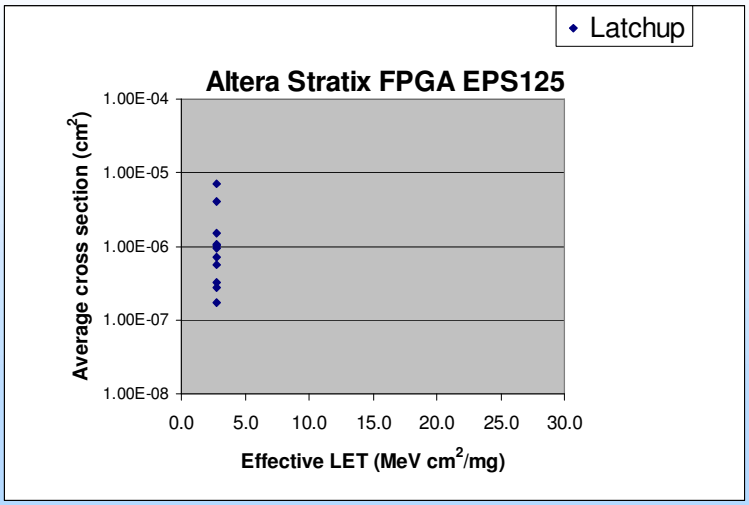
HEAVY ION TEST RESULTS

- The test evaluated the Altera Stratix EP1S25 using a Hyperterminal program
  - 115 kbps
  - 8 data bits
  - 1 stop bit
  - No parity
  - No hardware handshaking
- Nominal supply voltage was 5V to DUT Board's regulator, which released 3.3V to the DUT Board components
- Labview software was used to control power and monitor current as well as capture error waveforms
- The Altera Stratix EP1S25 experienced SEFIs before Single Event Latchup (SEL) occurred at an LET of 2.8 MeV/(mg/cm^2)

DATA COLLECTED

DUT #	Angle (Degrees)	Effective LET (MeV-cm^2/mg	Latchup Events	Cross Section (cm^2)
1	0	2.8	1	5.65E-07
1	0	2.8	1	1.08E-06
1	0	2.8	1	2.77E-07
1	0	2.8	1	7.14E-07
1	0	2.8	1	1.70E-07
1	0	2.8	1	9.43E-07
2	0	2.8	1	1.49E-06
2	0	2.8	1	3.23E-07
2	0	2.8	1	1.04E-06
2	0	2.8	1	7.04E-06
2	0	2.8	1	4.02E-06

LATCHUP CURVE



SUMMARY

- Heavy Ion Testing
  - Two ALTERA Stratix EP1S25 experienced SEL conditions at an LET of 2.8 MeV/(mg/cm^2)
  - The devices were exposed from a fluence of 1.42 x 10^5 to 3.10 x 10^6 particles/cm^2 of Neon
  - The test consisted of eleven exposure runs at the minimum specified operating voltage of 3.3V converted from a 5 volt regulator
  - Both devices were tested with the FPGA programmed with a binary counting pattern
  - SEL

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SPONSORS

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